03-03-03

RCE/2800

PTO/SB/30 (10/01)

REQUEST FOR CONTINUED EXAMINATION (RCE) TRANSMITTAL

Address to:
Commissioner for Patents
Box RCE
Washington, DC 20231

Application Number	09/742,204
Filing Date	December 20, 2000
First Named Inventor	Glen FOX
Group Art Unit	2823
Examiner Name	Khiem D. NGUYEN
Attorney Docket Number	FUJ00-01013 RAM

#13/RCE Appeal 3/12/03

This is a Request for Continued Examination (RCE) under 37 C.F.R. 1.114 of the above-identified application.

NOTE: If the above-identified application was filed prior to May 29, 2000, applicant may wish to consider filing a continued prosecution application (CPA) under 37 C.F.R. 1.53(d) (PTO/SB/29) instead of a RCE to be eligible for the patent term adjustment provisions of the AIPA. See Changes to Application Examination and Provisional Application Practice, Final Rule, 65 Fed. Reg. 50092 (Aug. 16, 2000); Interim Rule, 65 Fed. Reg. 14865 (Mar. 20, 2000), 1233 Off. Gaz. Pat. Office 47 (Apr. 11, 2000), which established RCE Pratice..

1. Submission required under 37 C.F.R. 1.114
   - a. ☐ Previously submitted
     - i. ☐ Consider the amendment(s)/reply under 37 C.F.R. 1.116 previously filed on _____ (Any unentered amendment(s) referred to above will be entered).
     - ii. ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____
     - iii. ☐ Other _____
   - b. ☒ Enclosed
     - i. ☒ Amendment/Reply and Petition for 1-Month Extension
     - ii. ☐ Affidavit(s)/Declaration(s)
     - iii. ☐ Information Disclosure Statement (IDS), Form SB/08A and copy of Reference
     - iv. ☐ Other _____

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2. Miscellaneous
   - a. ☐ Suspension of action on the above-identified application is requested under 37 C.F.R. 1.103(c) for a period of _____ months. (Period of suspension shall not exceed 3 months; Fee under 37 C.F.R. 1.17(i) **required**)
   - b. ☐ Other

3. Fees The RCE fee under 37 C.F.R. 1.17(e) is required by 37 C.F.R. 1.114 when the RCE is filed.
   - a. ☒ The Director is hereby authorized to charge the following fees, or credit any overpayments, to Deposit Account No. 50-1123
     - i. ☐ RCE fee required under 37 C.F.R 1.17(e)
     - ii. ☐ Extension of time fee (37 C.F.R 1.136 and 1.17)
     - iii. ☒ Other: Charge any additional fees or credit any overpayments **for this filing**
   - b. ☒ Check in the amount of $860.00 enclosed
   - c. ☐ Payment by credit card (Form PTO-2038 enclosed)

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

Name (Print/Type)	Carol W. Burton	*Registration No. (Attorney/Agent)*	35,465
Signature		*Date*	February 27, 2003

CERTIFICATE OF MAILING OR TRANSMISSION

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Attorney Docket No. FUJ00-01013 RAM
Client/Matter No. 80458.0007

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re U.S. Application of:	
Glen FOX	Examiner: Khiem D. NGUYEN
Serial No. 09/742,204	Art Unit: 2823
Filed: December 20, 2000	
For: PROCESS FOR PRODUCING HIGH QUALITY PZT FILMS FOR FERROELECTRIC MEMORY INTEGRATED CIRCUITS	

#14/Arnold D. Appeal 8/12/03

AMENDMENT ACCOMPANYING RCE TRANSMITTAL

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

In response to the Final Office Action mailed November 6, 2002, and in support of the Request for Continued Examination filed herewith, please enter the following amendments and consider the remarks which follow.

IN THE CLAIMS:

Please amend claims 1, 12, 27 and 30 according to the attached sheets.

REMARKS

Claims 1 and 4 stand rejected under 35 USC 103(a) as being unpatentable over the applicant's admitted prior art (AAPA) in view of *Miyazawa et al* (US Patent No. 5,953,619) and *Evans et al* (US Patent 6,150,184).

Claims 2-3 and 5-11 stand rejected under 35 USC 103(a) as being unpatentable over the AAPA in view of *Miyazawa et al* and *Evans et al*, and further in view of *Joshi et al* (US Patent No. 6,322,849) and *Van Buskirk et al* (US Patent No. 6,316,797).

Claims 12-17 and 19-24 stand rejected under 35 USC 103(a) as being unpatentable over the AAPA in view of *Miyazawa et al* and *Otto et al* (US Patent No. 6,284,712).

Claims 27-31 stand rejected under 35 USC 103(a) as being unpatentable over the AAPA in view of *Miyazawa et al* and *Van Buskirk et al.*

The rejections of claims 1-17, 19-24, and 27-31 as now amended and as set forth above under 35 USC 103(a) are respectfully traversed. The rejections of each of the claim sets are addressed in turn.

A. *Miyazawa* Fails To Teach Or Suggest A First Anneal That Changes The Ferroelectric Dielectric Material To A Perovskite Phase Before The Top Electrode Is Formed, And A Second Anneal That Further Changes The Ferroelectric Dielectric Material To Have A Columnar Structure After The Top Electrode.

The Examiner has cited *Miyazawa et al* for the proposition that after the PZT dielectric film 28 is deposited and before or after the upper electrode layer 29 is deposited, an annealing process in an O_2 atmosphere is performed (col. 4, line 66 to col. 5, line 1).

However, *Miyazawa et al* teaches that this annealing process in an O_2 atmosphere polycrystallizes the PZT dielectric film 28 (col. 5, lines 9-10). *Miyazawa et al* does not teach two important limitations that are now found in each of independent claims 1, 12, 27, and 30:

As amended, claims 1, 12, 27, and 30 each now recite:

> annealing the layer of ferroelectric dielectric material to form perovskite phases with a first anneal.

As amended, claims 1 and 12, as well as previous claims 27 and 30 recite:

> annealing the layer of ferroelectric dielectric material with a second anneal, the second anneal changing the layer of ferroelectric material into grains having a columnar structure and performed after the step of deposition of an electrically conductive top electrode layer.

No new matter has been added by the claim amendments herein, for which support is found in the specification at page 5, lines 5-7, as well as in the claims as previously filed.

All independent claims now claim a first anneal that changes the ferroelectric dielectric material to a perovskite phase before the top electrode is formed, and a second anneal that further changes the ferroelectric dielectric material to have a columnar structure after the top electrode is formed. These limitations in the sequence claimed are neither shown nor suggested by *Miyazawa et al.* or the admitted prior art (AAPA).

B. *Evans* Fails To Teach Or Suggest A First Anneal And A Second Anneal Performed Before And After The Top Electrode Formation.

Evans et al teaches that a second anneal can be performed after the top electrodes 22 are etched. *Evans et al* neither teaches nor suggests that a first anneal and a second anneal are performed before and after the top electrode formation as now claimed.

Since neither the *Miyazawa et al* reference nor the *Evans et al* reference singly teach the limitations found in claim 1, the combination also fails to teach or suggest the limitations of claim 1, as now amended. Claim 1 is thus patentably distinguishable over the combination of the cited references and allowable under 35 USC 103(a). Additionally, claims 2-11 are believed to be allowable as depending from an allowable base claim.

C. *Otto* Fails To Teach Or Suggest The Formation Of A Perovskite Phase As Now Claimed Prior To The Top Electrode Formation.

Otto et al is cited for the proposition that a first and second anneal is performed in an environment comprising a mixture of oxygen and inert gas. However, *Otto et al* is silent regarding the formation of a perovskite phase as now claimed prior to the top electrode formation. For the reasons given above with respect to the combination of the *Miyazawa et al* and *Evans et al* references, claim 12 is also believed patentable over the combination of *Miyazawa et al* and *Otto et al.* Additionally, claims 13-17 and 19-24 are also believed allowable as depending from an allowable base claim.

D. *Van Buskirk* Fails To Teach Or Suggest The Formation Of A Perovskite Phase As Now Claimed Prior To The Top Electrode Formation.

Van Buskirk et al is cited for an iridium oxide top electrode. However, *Van Buskirk et al* is silent regarding the formation of a perovskite phase as now claimed prior to the top electrode formation. For the reasons given above with respect to the combination of *Miyazawa et al* and *Evans et al.*, claims 27 and 30 are also believed patentable over the combination. Additionally, claims 28-29 and 31 are believed allowable as depending from an allowable base claim.

E. Conclusion.

For these reasons, pending claims 1-17, 19-24, and 27-31 are now believed fully allowable over the combination of cited references, and the case is in condition for allowance.

Should any issues remain, the Examiner is kindly asked to the telephone the undersigned.

Respectfully submitted,

February 27, 2003

Carol W. Burton, Reg. No. 35,465
Hogan & Hartson L.L.P.
1200 17th Street, Suite 1500
Denver, Colorado 80202
Telephone: (303) 454-2454
Facsimile: (303) 899-7333

MARKED-UP COPY OF AMENDED CLAIMS

1. (Twice Amended) A method for fabrication of ferroelectric capacitor elements of an integrated circuit comprising the steps of:

deposition of an electrically conductive bottom electrode layer;

deposition of a layer of ferroelectric dielectric material;

annealing the layer of ferroelectric dielectric material to form perovskite phases with a first anneal;

deposition of an electrically conductive top electrode layer;

annealing the layer of ferroelectric dielectric material with a second anneal, the second anneal changing the layer of ferroelectric material into grains having a columnar structure, being performed by rapid thermal annealing and performed after the step of deposition of an electrically conductive top electrode layer;

etching the electrically conductive top electrode layer; and

annealing the layer of ferroelectric dielectric material with another anneal after etching the electrically conductive top electrode layer.

12. (Twice Amended) A method for fabrication of ferroelectric capacitor elements of an integrated circuit comprising the steps of:

deposition of an electrically conductive bottom electrode layer comprising a noble metal;

deposition of a layer of ferroelectric dielectric material;

annealing the layer of ferroelectric dielectric material to form perovskite phases with a first anneal;

deposition of an electrically conductive top electrode layer comprising a noble metal oxide; and

annealing the layer of ferroelectric dielectric material with a second anneal, the second anneal changing the layer of ferroelectric material into grains having a columnar structure, being performed in an environment comprising a mixture of oxygen and inert gas, the oxygen having partial pressure of less than five percent of one atmosphere and

performed after the step of deposition of an electrically conductive top electrode layer.

27. (Amended) A method for fabrication of ferroelectric capacitor elements of an integrated circuit comprising the steps of:

deposition of an electrically conductive bottom electrode layer;

deposition of a layer of ferroelectric dielectric material by a sputtering method;

annealing the layer of ferroelectric dielectric material to form perovskite phases with a first anneal;

deposition of an electrically conductive top electrode layer; and

annealing the layer of ferroelectric dielectric material with a second anneal, the second anneal changing the layer of ferroelectric material into grains having a columnar structure and performed after the step of deposition of an electrically conductive top electrode layer.

30. (Amended) A method for fabrication of ferroelectric capacitor elements of an integrated circuit comprising the steps of:

deposition of an electrically conductive bottom electrode layer;

deposition of a layer of ferroelectric dielectric material;

annealing the layer of ferroelectric dielectric material to form perovskite phases with a first anneal;

deposition of an electrically conductive top electrode layer comprising amorphous iridium oxide; and

annealing the layer of ferroelectric dielectric material with a second anneal, the second anneal changing the layer of ferroelectric material into grains having a columnar structure and performed after the step of deposition of an electrically conductive top electrode layer.

CLEAN COPY OF AMENDED CLAIMS

1. (Twice Amended) A method for fabrication of ferroelectric capacitor elements of an integrated circuit comprising the steps of:

deposition of an electrically conductive bottom electrode layer;

deposition of a layer of ferroelectric dielectric material;

annealing the layer of ferroelectric dielectric material to form perovskite phases with a first anneal;

deposition of an electrically conductive top electrode layer;

annealing the layer of ferroelectric dielectric material with a second anneal, the second anneal changing the layer of ferroelectric material into grains having a columnar structure, being performed by rapid thermal annealing and performed after the step of deposition of an electrically conductive top electrode layer;

etching the electrically conductive top electrode layer; and

annealing the layer of ferroelectric dielectric material with another anneal after etching the electrically conductive top electrode layer.

12. (Twice Amended) A method for fabrication of ferroelectric capacitor elements of an integrated circuit comprising the steps of:

deposition of an electrically conductive bottom electrode layer comprising a noble metal;

deposition of a layer of ferroelectric dielectric material;

annealing the layer of ferroelectric dielectric material to form perovskite phases with a first anneal;

deposition of an electrically conductive top electrode layer comprising a noble metal oxide; and

annealing the layer of ferroelectric dielectric material with a second anneal, the second anneal changing the layer of ferroelectric material into grains having a columnar structure, being performed in an environment comprising a mixture of oxygen and inert gas, the oxygen having partial pressure of less than five percent of one atmosphere and

performed after the step of deposition of an electrically conductive top electrode layer.

27. (Amended) A method for fabrication of ferroelectric capacitor elements of an integrated circuit comprising the steps of:

deposition of an electrically conductive bottom electrode layer;

deposition of a layer of ferroelectric dielectric material by a sputtering method;

annealing the layer of ferroelectric dielectric material to form perovskite phases with a first anneal;

deposition of an electrically conductive top electrode layer; and

annealing the layer of ferroelectric dielectric material with a second anneal, the second anneal changing the layer of ferroelectric material into grains having a columnar structure and performed after the step of deposition of an electrically conductive top electrode layer.

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deposition of an electrically conductive bottom electrode layer;

deposition of a layer of ferroelectric dielectric material;

annealing the layer of ferroelectric dielectric material to form perovskite phases with a first anneal;

deposition of an electrically conductive top electrode layer comprising amorphous iridium oxide; and

annealing the layer of ferroelectric dielectric material with a second anneal, the second anneal changing the layer of ferroelectric material into grains having a columnar structure and performed after the step of deposition of an electrically conductive top electrode layer.